CpEG 315-11 Digital Systems Design II With Laboratory
Fall 2014, Tuesday and Thursday 11:00AM-12:15PM

Instructor: Miad Faezipour
Email: mfaezipo@bridgeport.edu
Office: Technology Building-Room 155
Office Hours: Wednesdays 3:00-5:00pm or by appointment
Teaching Assistant: To be announced

Credit Hours:
4 semester hours: 3 Lecture hours and 1 Lab hour
CpEG 315 is a 4 credit hours course. For each of the four credit hours, there is one hour of classroom/laboratory or direct faculty instruction and a minimum of two hours of out of class student work each week for approximately fifteen weeks for one semester.

Pre-requisites:
CpEG 210 or equivalent
Debugging Experience with some high level programming language

Required References:
2. Class Notes and Class Webpage: Canvas www.bridgeport.edu/myub

Other References:
3. Rapid Prototyping of Digital Systems: SOPC Ed (w/CD), by Hamblen
8. An Engineering Approach to Digital Design, by Fletcher

Course Description:
This course familiarizes students with the design of complex digital systems; mainly top-down design and modularization, Implementation of controllers, Use of hardware design languages (Verilog/VHDL) to implement systems, Rapid prototyping, and Fault tolerant design. The lab includes implementation of digital systems using FPGAs.

Course Objectives:
Learn methodologies to design large digital systems
Use Verilog to implement designs
Target programmable logic
Use a variety of instrumentation and tools to implement and debug designs
Policies:
1. All classes will be conducted as per the university regulations.
2. Extensive computer work will be required for programming assignments and labs. The class will use Altera Boards, Quartus II and/or ModelSim/Synopsys synthesis and simulation CAD tools.
3. Homework assignments will be assigned regularly on a weekly basis. The ten best homework sets will be counted toward the final course grade.
4. Copying is strictly prohibited. All assignments must be individual works. Cheating in assignments/exams/projects will result in automatic F grade.
5. Assignments are due in the first 30 minutes of the class after which it is considered late. Late assignments are not accepted at all.
6. Solutions to the homeworks will be supplied.
7. Graded work must be disputed within 10 days after it is returned to the students.
8. Special requests must be made well ahead of time. Explicit permission of the instructor will be required for such cases.
9. Several laboratory assignments will emphasize the practical aspects of the course. Designs will be implemented using programmable logic. Diagnostic equipment including oscilloscopes, logic analyzers and power supplies will be used to troubleshoot the resulting circuits. Formal written reports (using a word processor) will be required for all labs using a format to be presented. A final term project may also require an oral presentation.
10. Laboratory site is Tech 211B. Students will have access to the lab in the designated lab hours (Tuesdays 5:00pm-7:30PM).
11. Regular attendance is recommended. Students are expected to log on to the Canvas class webpage www.bridgeport.edu/myub frequently in order find any current postings. You can get a UB email account by going to: www.bridgeport.edu/ubnet.

Grading Policy:
Following is the tentative grading policy:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Homeworks</td>
<td>10%</td>
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<tr>
<td>Labs and Miniprojects</td>
<td>15%</td>
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<tr>
<td>Midterm Test 1</td>
<td>15%</td>
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<tr>
<td>Midterm Test 2</td>
<td>15%</td>
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<tr>
<td>Final Project</td>
<td>15%</td>
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<tr>
<td>Final Test</td>
<td>30%</td>
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Lecture Topics (Tentative):
1. Review of Basic Digital Design
   a) Combinational design - gates (K-maps), MSI (muxes, decoders et al)
   b) Sequential design - FFs, basic methodology, Mealy and Moore machines
2. Design methodologies
   a) Top-down design
   b) Modular building blocks - controller and architecture (data path)
   c) Algorithmic state machines (ASMs)
   d) Timing diagrams in sequential design
   e) Simulation using computer tools
   f) Descriptive methodologies - structural, behavioral, dataflow (review)
3. Verilog (review)
   a) Basic design features
   b) Structural design vs. schematic capture
   c) Altera tool set (Quartus II)
   d) Various primitives – the always block, if-else, case, for loop et al
4. Controller design
   a) Multiplexer method
b) One-hot method  
c) ROM-based implementation and other memory systems  
d) Implementations using PLAs and PALs  
e) Special considerations and guidelines  
f) Design examples – networks with arithmetic operations

5. More Verilog  
a) Behavioral descriptions and modeling  
b) Behavioral and dataflow descriptions  
c) More primitives  
d) Blocking and non-blocking assignment  
e) Data types - scalar and composite  
f) Sequential control statements  
g) Task and functions  
h) Verilog modeling techniques for combinational and sequential logic  
i) Arithmetic networks and their implementation

6. Microprogrammed design  
a) Microprogramming examples  
b) Single and multiple qualifiers per state  
c) Microinstruction format - horizontal vs. vertical  
d) Microcontrollers  
e) Bit-slice implementation - AMD 2909 and 2910, newer bit-slice devices  
f) Microprogrammed design and Verilog  
g) Linked state machines

7. Case Studies – Floating point logic and additional modeling with Verilog

8. Design for Testability  
a) Scan techniques  
b) Fault models  
c) Boundary scan  
d) Built-in self-test (BIST)

9. Laboratories  
a) Describe and simulate a multiplexer in Verilog using Quartus  
b) Introduction to the Altera DE2 board  
c) Design, simulate and implement a vending machine on the DE2 board (state machines)  
d) More I/O and state machines  
e) VGA monitor interface the DE2 board with a  
f) Mouse interface to the DE2 board and sprites  
g) Final project

Important Dates:  
Holiday(s): Thursday, Nov. 27, 2014 – Thanksgiving Holiday  
Midterm Test 1: Thursday, Oct. 16, 2014 – 11:00am-12:15pm.  
Midterm Test 2: Thursday, Nov. 13, 2014 – 11:00am-12:15pm.  

*Note: These descriptions and timelines are subject to change at the discretion of the Instructor.